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**EE 4513 VLSI**

**Report Lab 10**

**November 6, 2019**

For this lab, I created a Single Precision Floating Point Adder with the help of lots of research papers and schematics, I was able to make a successful working IEEE single floating-point adder. It was difficult and challenging, with pipelines I was able to make one module and work with it. At the end everything came out pretty good.

Fall 2019

# EE 4513 – Introduction to VLSI Design

**Lab Assignment # 10**

In this lab assignment,

1. You are required to design: (i) IEEE Single Precision Floating Point Adder.

1. Once you have completed the behavioral simulation (for example, using Vivado), synthesize your code to generate the netlist using Cadence RTL Compiler (RC).

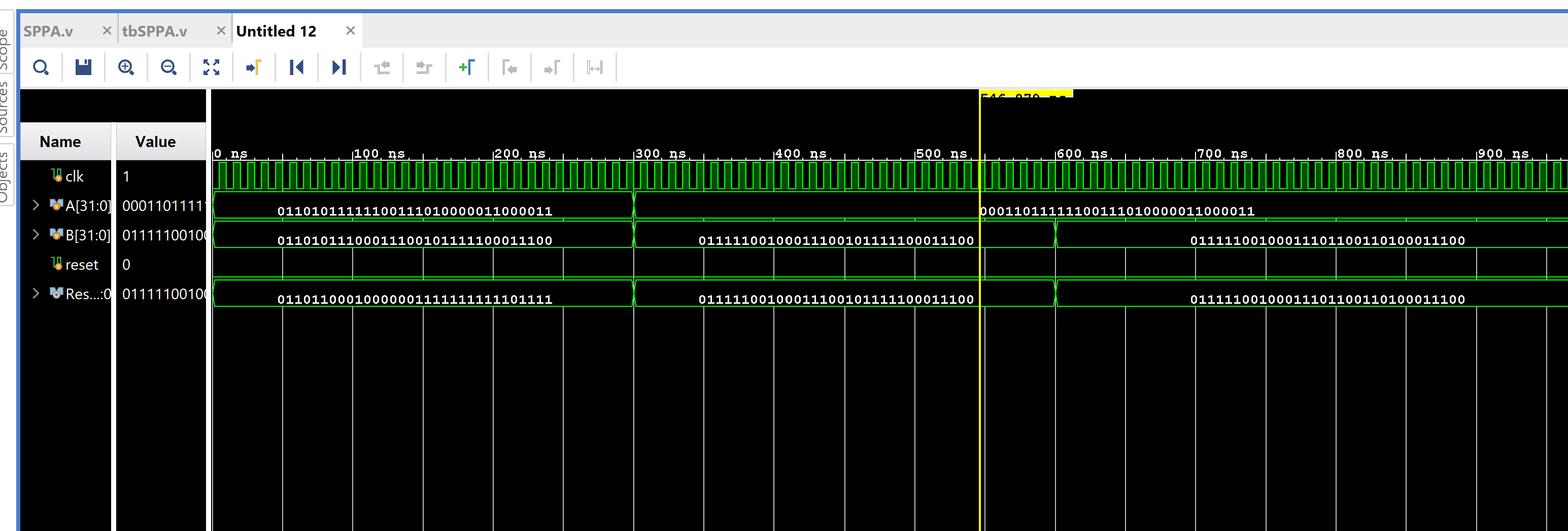
1. Then, use the Cadence Encounter platform to generate the schematic and GDS2 layout of your design. Verify your design for connectivity, and geometry violations.

Turn in report, which includes the following: -

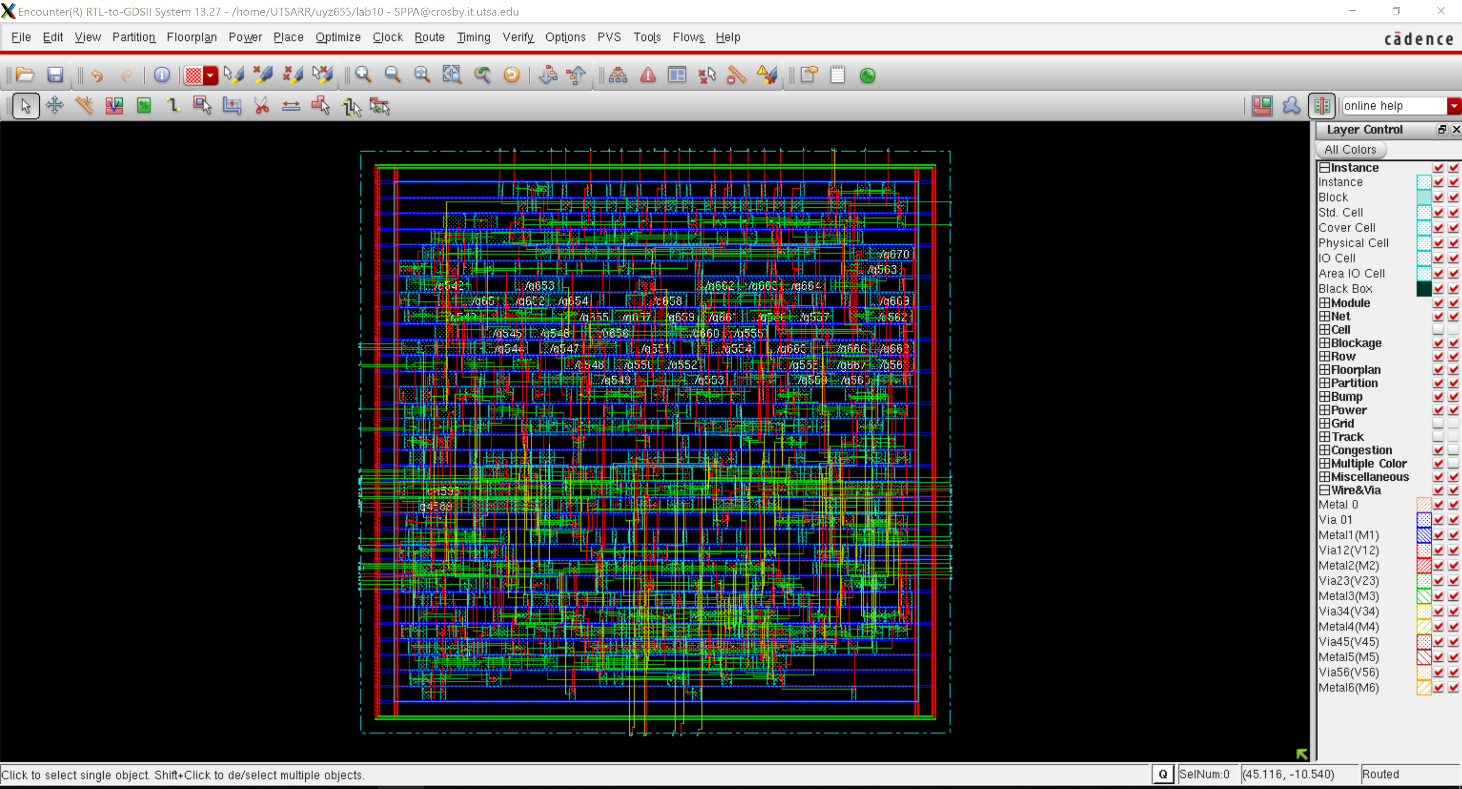
* 1. Verlog Code and Simulation waveforms for your FP unit

module SPPA(input clk, input reset, input [31:0]A, input [31:0]B, output [31:0]Result);

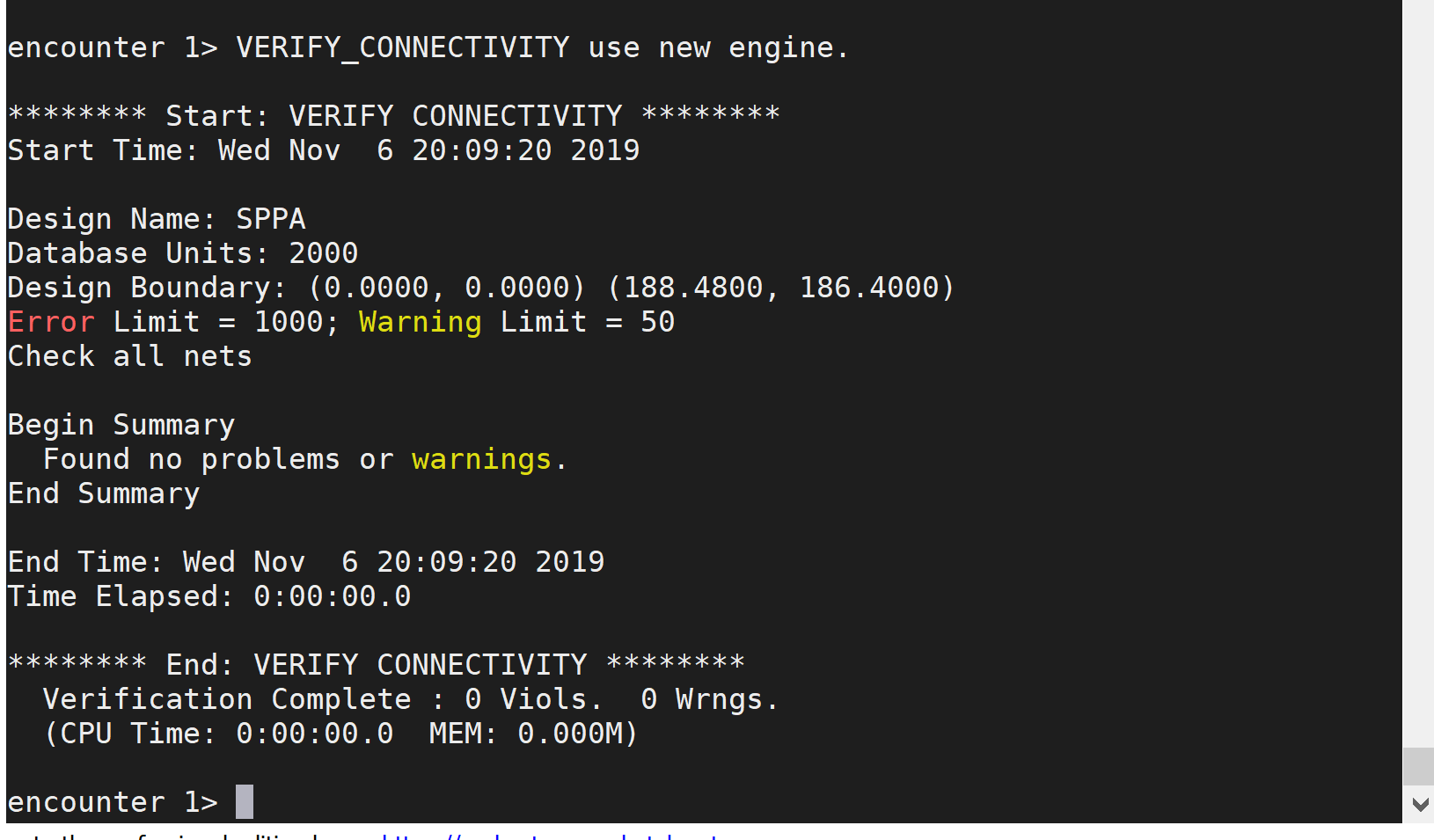
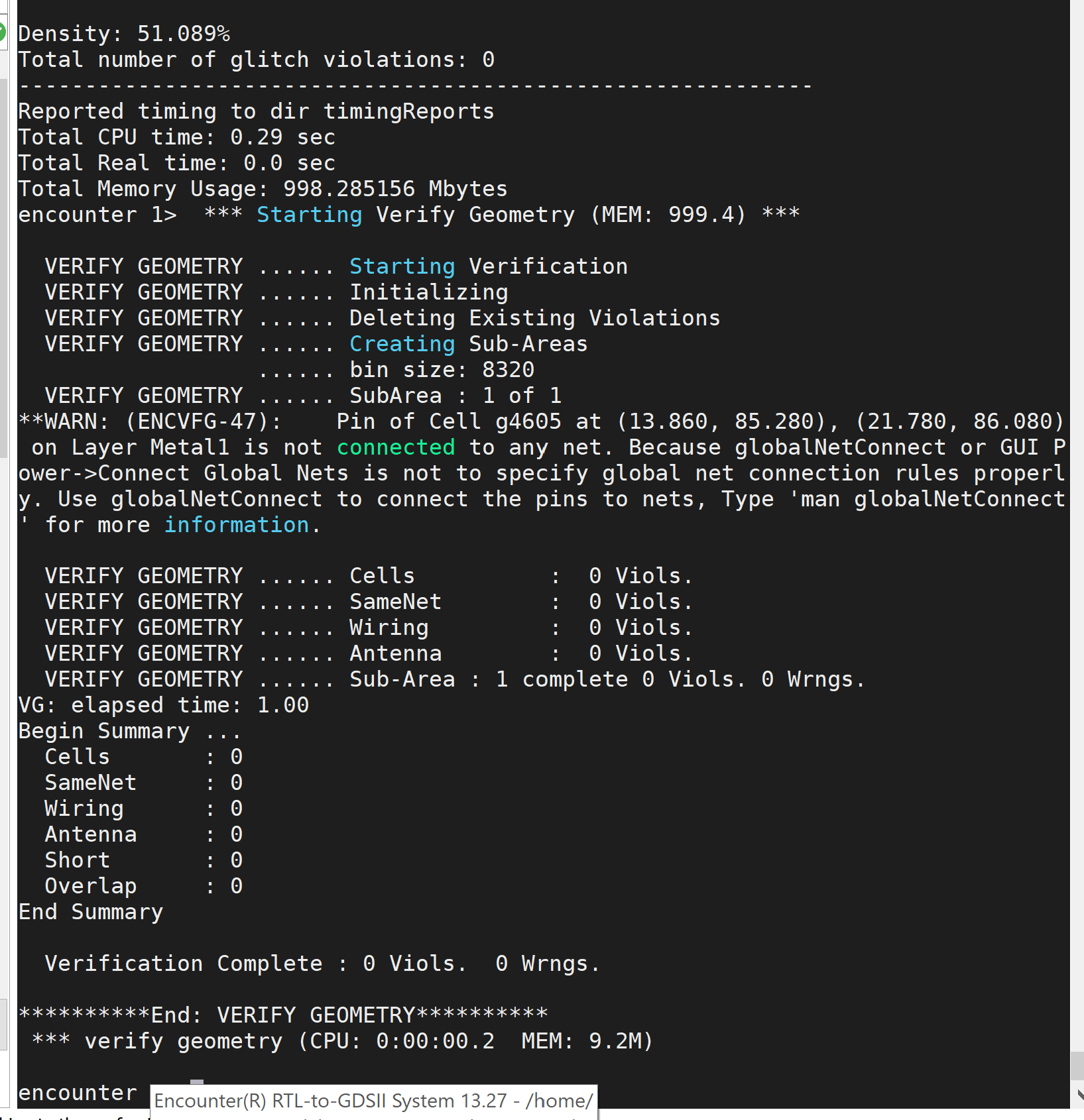
* 2. reg [31:0] Num\_shift;
  3. reg [7:0] Larger\_exp,Final\_expo;
  4. reg [22:0] Small\_exp\_ma,S\_mantissa,L\_mantissa,Large\_ma,Final\_mant;
  5. reg [23:0] Add\_mant,Add1\_mant;
  6. reg [7:0] e1,e2;
  7. reg [22:0] m1,m2;
  8. reg s1,s2,Final\_sign;
  9. reg [3:0] renorm\_shift;
  10. integer signed renorm\_exp;
  11. reg [31:0] Result1;
  12. assign Result = Result1;
  13. always @(\*) begin
  14. e1 = A[30:23];
  15. e2 = B[30:23];
  16. m1 = A[22:0];
  17. m2 = B[22:0];
  18. s1 = A[31];
  19. s2 = B[31];
  21. if (e1 > e2) begin
  22. Num\_shift = e1 - e2;
  23. Larger\_exp = e1;
  24. Small\_exp\_ma = m2;
  25. Large\_ma = m1;
  26. end
  28. else begin
  29. Num\_shift = e2 - e1;
  30. Larger\_exp = e2;
  31. Small\_exp\_ma = m1;
  32. Large\_ma = m2;
  33. end
  34. if (e1 == 0 | e2 ==0) begin
  35. Num\_shift = 0;
  36. end
  37. else begin
  38. Num\_shift = Num\_shift;
  39. end
  41. if (e1 != 0) begin
  42. Small\_exp\_ma = {1'b1,Small\_exp\_ma[22:1]};
  43. Small\_exp\_ma = (Small\_exp\_ma >> Num\_shift);
  44. end
  45. else begin
  46. Small\_exp\_ma = Small\_exp\_ma;
  47. end
  48. if (e2!= 0) begin
  49. Large\_ma = {1'b1,Large\_ma[22:1]};
  50. end
  51. else begin
  52. Large\_ma = Large\_ma;
  53. end
  54. if (Small\_exp\_ma < Large\_ma) begin
  55. S\_mantissa = Small\_exp\_ma;
  56. L\_mantissa = Large\_ma;
  57. end
  58. else begin
  60. S\_mantissa = Large\_ma;
  61. L\_mantissa = Small\_exp\_ma;
  62. end
  64. if (e1!=0 & e2!=0) begin
  65. if (s1 == s2) begin
  66. Add\_mant = S\_mantissa + L\_mantissa;
  67. end else begin
  68. Add\_mant = L\_mantissa - S\_mantissa;
  69. end
  70. end
  71. else begin
  72. Add\_mant = L\_mantissa;
  73. end
  74. if (Add\_mant[23]) begin
  75. renorm\_shift = 4'd1;
  76. renorm\_exp = 4'd1;
  77. end
  78. else if (Add\_mant[22])begin
  79. renorm\_shift = 4'd2;
  80. renorm\_exp = 0;
  81. end
  82. else if (Add\_mant[21])begin
  83. renorm\_shift = 4'd3;
  84. renorm\_exp = -1;
  85. end
  86. else if (Add\_mant[20])begin
  87. renorm\_shift = 4'd4;
  88. renorm\_exp = -2;
  89. end
  90. else if (Add\_mant[19])begin
  91. renorm\_shift = 4'd5;
  92. renorm\_exp = -3;
  93. end
  94. Final\_expo = Larger\_exp + renorm\_exp;
  96. Add1\_mant = Add\_mant << renorm\_shift;
  97. Final\_mant = Add1\_mant[23:1];
  99. if (s1 == s2) begin
  100. Final\_sign = s1;
  101. end
  102. if (e1 > e2) begin
  103. Final\_sign = s1;
  104. end else if (e2 > e1) begin
  105. Final\_sign = s2;
  106. end
  107. else begin
  108. if (m1 > m2) begin
  109. Final\_sign = s1;
  110. end else begin
  111. Final\_sign = s2;
  112. end
  113. end
  115. Result1 = {Final\_sign,Final\_expo,Final\_mant};
  116. end
  118. always @(posedge clk) begin
  119. if(reset) begin
  120. Num\_shift <= #1 0;
  121. end
  122. end
  124. Endmodule

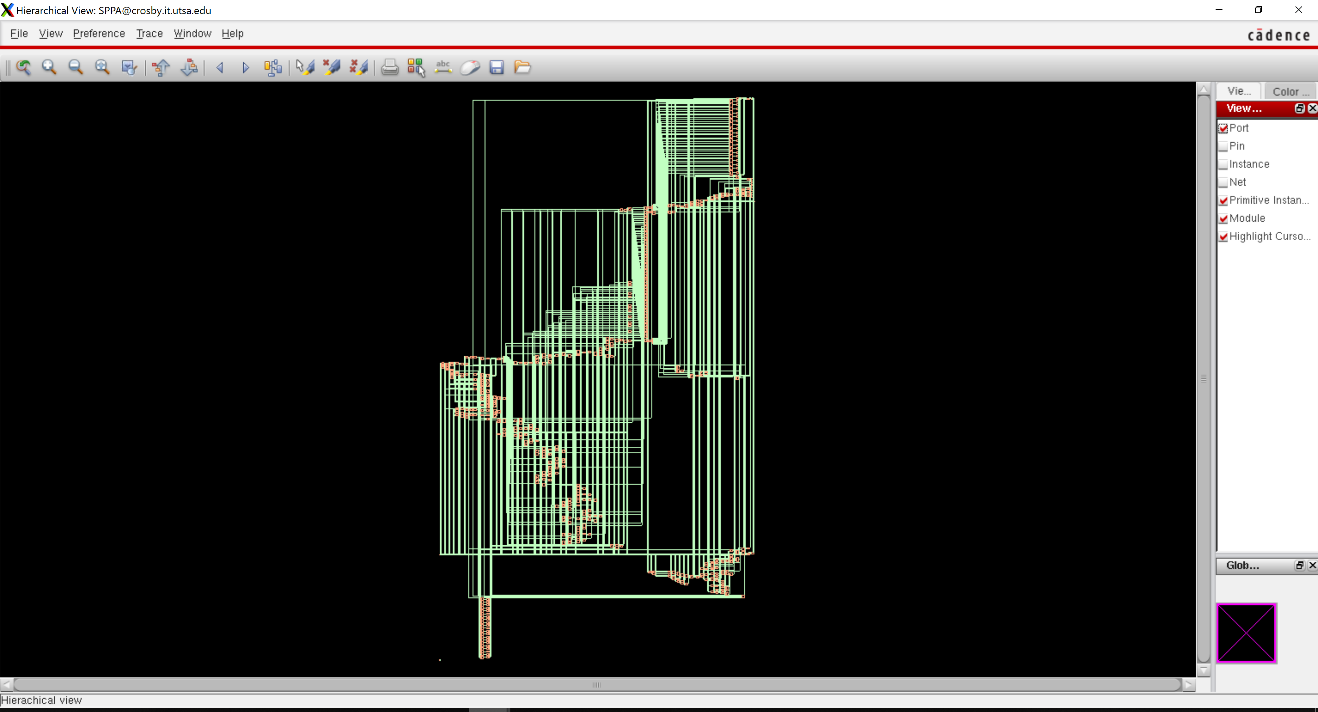


* 1. Physical Layout snapshot of your design



* 1. Snapshots of portions of the connectivity and geometry verification reports, showing any violations, if present.



* 1. Schematic of your design (can be seen by clicking Tools -> Schematic Viewer) 
  2. Report Your Timing Analysis (Slew, Delay, Arrival...etc) and Total Area from your RTL compiler for your design. ============================================================
  3. Generated by: Encounter(R) RTL Compiler RC13.12 - v13.10-s021\_1
  4. Generated on: Nov 06 2019 07:44:00 pm
  5. Module: SPPA
  6. Technology library: tsmc18 1.0
  7. Operating conditions: slow (balanced\_tree)
  8. Wireload mode: enclosed
  9. Area mode: timing library
  10. ============================================================
  11. Pin Type Fanout Load Slew Delay Arrival
  12. (fF) (ps) (ps) (ps)
  13. -------------------------------------------------------------------
  14. B[23] in port 4 10.7 0 +0 0 F
  15. g3035/AN +0 0
  16. g3035/Y NAND2BXL 4 11.6 185 +214 214 F
  17. g3007/A1 +0 214
  18. g3007/Y AOI21XL 3 9.3 363 +302 516 R
  19. g2998/A0 +0 516
  20. g2998/Y OAI21XL 3 7.5 182 +152 668 F
  21. g2995/A1N +0 668
  22. g2995/Y OAI2BB1XL 4 12.1 195 +285 952 F
  23. g2987/A0 +0 952
  24. g2987/Y AOI21XL 1 3.4 209 +190 1143 R
  25. g2985/A0 +0 1143
  26. g2985/Y OAI21XL 1 1.5 108 +89 1232 F
  27. g2984/A1N +0 1232
  28. g2984/Y OAI2BB1X1 36 111.2 940 +725 1957 F
  29. g2983/A +0 1957
  30. g2983/Y INVX1 34 113.5 1414 +1043 3000 R
  31. g2982/B +0 3000
  32. g2982/Y NAND2XL 5 16.7 396 +292 3292 F
  33. g2934/A0 +0 3292
  34. g2934/Y OAI22XL 19 62.6 1856 +1073 4365 R
  35. srl\_49\_36/SH[1]
  36. g1966/A +0 4365
  37. g1966/Y INVX1 20 70.2 749 +646 5010 F
  38. g1929/A +0 5010
  39. g1929/Y NAND2XL 4 14.2 364 +363 5374 R
  40. g1876/A0 +0 5374
  41. g1876/Y OAI222XL 1 3.5 226 +218 5592 F
  42. g1863/B0 +0 5592
  43. g1863/Y AOI211XL 1 2.6 293 +210 5802 R
  44. g1862/A +0 5802
  45. g1862/Y INVXL 1 3.4 87 +69 5871 F
  46. srl\_49\_36/Z[1]
  47. g6094/A0 +0 5871
  48. g6094/Y AOI22XL 3 10.5 492 +259 6130 R
  49. g6093/A +0 6130
  50. g6093/Y INVX1 2 5.6 119 +86 6216 F
  51. g6050/A0N +0 6216
  52. g6050/Y AOI2BB1XL 1 3.2 130 +250 6466 F
  53. g6045/B0 +0 6466
  54. g6045/Y AOI21XL 1 3.2 236 +152 6618 R
  55. g6043/B0 +0 6618
  56. g6043/Y AOI21XL 1 3.4 176 +78 6695 F
  57. g6034/A0 +0 6695
  58. g6034/Y AOI211XL 1 4.7 353 +294 6989 R
  59. g6222/C0 +0 6989
  60. g6222/Y AOI221X1 1 3.2 220 +95 7084 F
  61. g6032/B0 +0 7084
  62. g6032/Y AOI21XL 1 3.4 212 +174 7258 R
  63. g6031/C0 +0 7258
  64. g6031/Y AOI221XL 1 3.6 255 +90 7348 F
  65. g6030/A0 +0 7348
  66. g6030/Y OAI221XL 1 3.0 421 +244 7592 R
  67. g6029/B0 +0 7592
  68. g6029/Y OAI21XL 1 4.4 167 +153 7746 F
  69. g2/B +0 7746
  70. g2/Y NOR3BX1 1 3.2 221 +199 7944 R
  71. g6027/B0 +0 7944
  72. g6027/Y AOI21XL 1 3.5 177 +77 8021 F
  73. g6026/A0 +0 8021
  74. g6026/Y AOI33XL 1 3.4 389 +233 8254 R
  75. g6025/A0 +0 8254
  76. g6025/Y AOI22XL 1 3.5 216 +114 8369 F
  77. g6024/A0 +0 8369
  78. g6024/Y AOI31XL 2 6.3 325 +241 8610 R
  79. g6022/A0 +0 8610
  80. g6022/Y AOI21XL 1 3.5 149 +131 8741 F
  81. g6021/B0 +0 8741
  82. g6021/Y OAI2BB2XL 1 3.0 231 +181 8922 R
  83. g6020/B0 +0 8922
  84. g6020/Y OAI21XL 1 4.6 154 +129 9050 F
  85. g6019/A0 +0 9050
  86. g6019/Y AOI22X1 46 154.3 2958 +1691 10742 R
  87. g6018/A +0 10742
  88. g6018/Y INVX1 45 150.7 1388 +1245 11987 F
  89. g6016/A0 +0 11987
  90. g6016/Y OAI22XL 2 10.3 646 +532 12519 R
  91. sub\_79\_26/B[1]
  92. g681/A +0 12519
  93. g681/Y INVX1 1 6.8 148 +104 12622 F
  94. g670/B +0 12622
  95. g670/CO ADDFX2 1 6.2 145 +535 13158 F
  96. g669/CI +0 13158
  97. g669/CO ADDFX2 1 6.2 145 +349 13506 F
  98. g668/CI +0 13506
  99. g668/CO ADDFX2 1 6.2 145 +349 13855 F
  100. g667/CI +0 13855
  101. g667/CO ADDFX2 1 6.2 145 +349 14204 F
  102. g666/CI +0 14204
  103. g666/CO ADDFX2 1 6.2 145 +349 14553 F
  104. g665/CI +0 14553
  105. g665/CO ADDFX2 1 6.2 145 +349 14901 F
  106. g664/CI +0 14901
  107. g664/CO ADDFX2 1 6.2 145 +349 15250 F
  108. g663/CI +0 15250
  109. g663/CO ADDFX2 1 6.2 145 +349 15599 F
  110. g662/CI +0 15599
  111. g662/CO ADDFX2 1 6.2 145 +349 15947 F
  112. g661/CI +0 15947
  113. g661/CO ADDFX2 1 6.2 145 +349 16296 F
  114. g660/CI +0 16296
  115. g660/CO ADDFX2 1 6.2 145 +349 16645 F
  116. g659/CI +0 16645
  117. g659/CO ADDFX2 1 6.2 145 +349 16994 F
  118. g658/CI +0 16994
  119. g658/CO ADDFX2 1 6.2 145 +349 17342 F
  120. g657/CI +0 17342
  121. g657/CO ADDFX2 1 6.2 145 +349 17691 F
  122. g656/CI +0 17691
  123. g656/CO ADDFX2 1 6.2 145 +349 18040 F
  124. g655/CI +0 18040
  125. g655/CO ADDFX2 1 6.2 145 +349 18388 F
  126. g654/CI +0 18388
  127. g654/CO ADDFX2 1 6.2 145 +349 18737 F
  128. g653/CI +0 18737
  129. g653/CO ADDFX2 1 6.2 145 +349 19086 F
  130. g652/CI +0 19086
  131. g652/CO ADDFX2 1 6.2 145 +349 19434 F
  132. g651/CI +0 19434
  133. g651/CO ADDFX2 3 9.1 154 +360 19794 F
  134. g649/A0 +0 19794
  135. g649/Y AOI22XL 3 8.3 420 +241 20035 R
  136. g648/B0 +0 20035
  137. g648/Y OAI2BB1XL 1 3.0 118 +92 20127 F
  138. g646/B0 +0 20127
  139. g646/Y OAI21XL 1 3.1 247 +104 20232 R
  140. sub\_79\_26/Z[23]
  141. g4681/B1 +0 20232
  142. g4681/Y AOI22XL 2 6.6 494 +174 20405 F
  143. g4680/A +0 20405
  144. g4680/Y INVX1 3 9.6 200 +196 20601 R
  145. g4628/B +0 20601
  146. g4628/Y NOR2XL 3 8.9 134 +124 20725 F
  147. g4623/A +0 20725
  148. g4623/Y AND2X1 3 8.9 119 +238 20963 F
  149. g4622/A +0 20963
  150. g4622/Y AND2X1 2 7.3 104 +225 21188 F
  151. g4620/B0 +0 21188
  152. g4620/Y AOI21XL 1 2.6 189 +136 21325 R
  153. g4619/A +0 21325
  154. g4619/Y INVXL 1 3.9 76 +67 21391 F
  155. renorm\_exp\_reg[1]/D TLATX1 +0 21391
  156. renorm\_exp\_reg[1]/G setup 0 +183 21574 R
  157. -------------------------------------------------------------------
  158. Timing slack : UNCONSTRAINED
  159. Start-point : B[23]
  160. End-point : renorm\_exp\_reg[1]/D

============================================================

Generated by: Encounter(R) RTL Compiler RC13.12 - v13.10-s021\_1

Generated on: Nov 06 2019 07:44:00 pm

Module: SPPA

Technology library: tsmc18 1.0

Operating conditions: slow (balanced\_tree)

Wireload mode: enclosed

Area mode: timing library

============================================================

Instance Cells Cell Area Net Area Total Area Wireload

-------------------------------------------------------------------

SPPA 778 13964 0 13964 <none> (D)

sub\_79\_26 53 1726 0 1726 <none> (D)

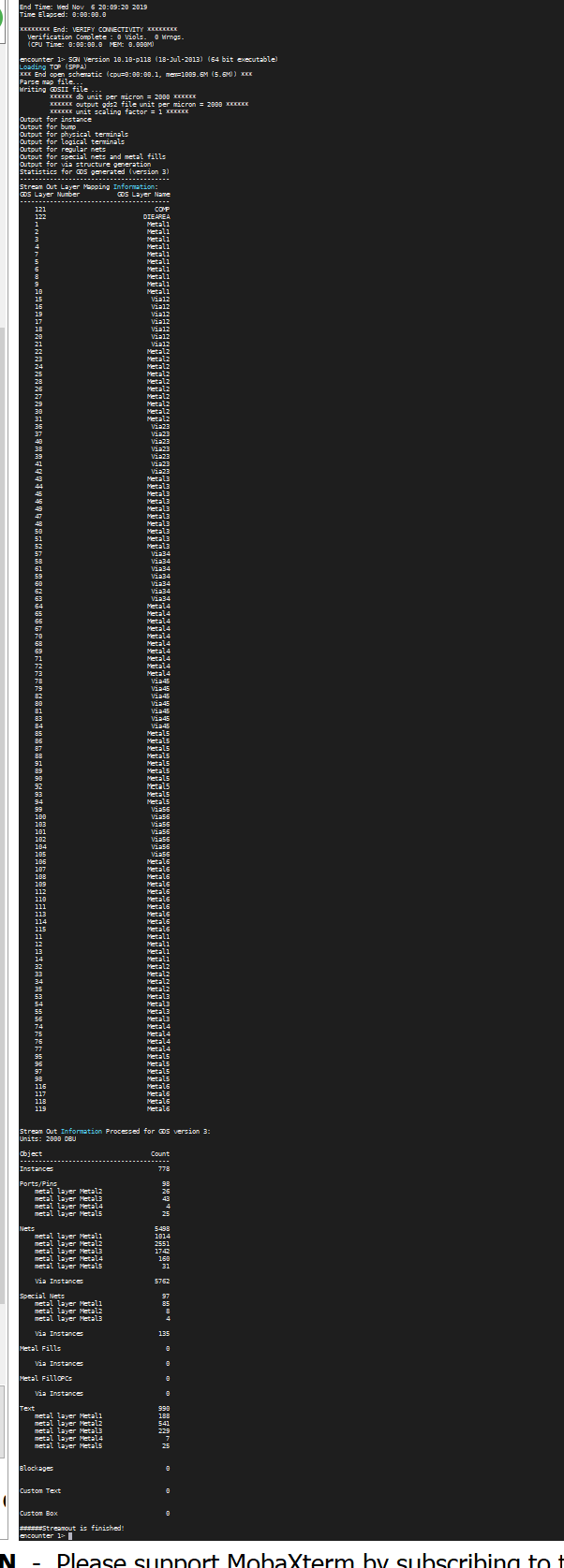
srl\_49\_36 108 1713 0 1713 <none> (D)

add\_77\_33 23 1573 0 1573 <none> (D)

sll\_109\_23 89 1347 0 1347 <none> (D)

(D) = wireload is default in technology library

* 1. Snapshot of the message showing successful generation of GDS2 layout



* 1. Try to optimize your design in the Verilog (efficient /structured code) and post a conclusion for your design.

**Note**: -

* 1. Once you have logged in, make a new directory called **lab10**. For example, if your account is abc.123, then upon login you will be taken to a directory with the same name. This is **your** home directory (not to be confused with another directory with the name ‘home’). To view the path of this directory, use the ‘pwd’ command. Then make the ‘lab10’ directory by using the **mkdir** command (**mkdir lab10**). Then change over to the lab10 directory using **cd lab10.** All the files related to this assignment should be in this directory. You must use the same names as mentioned here.
  2. In your report, you should clearly mention the file names that you choose for the various reports that are generated (verification, GDS2 etc.) while using Encounter.